

DESCRIPTION

Aries 3 is a fully programmable multimedia processor designed specifically for digital video applications such as DVD players, network clients, set-top boxes, and other convergence products. Based on VM Labs proven Aries architecture, Aries 3 delivers an unparalleled 3000 MIPS peak processing power that enables powerful new video entertainment features to differentiate and enhance consumer products.

VM Labs proprietary DVDplus Firmware transforms Aries 3 into the Aries 3 DVD Decoder, a state-of-the-art DVD decode IC that delivers the best playback performance and feature-set available. With DVDplus, the Aries 3 DVD Decoder is fully compatible with DVD Video, DVD Audio, VCD, CD, HDCD, and CDROM (MP3 encode/decode). To ensure the lowest possible system cost, the Aries 3 DVD Decoder performs multiple system functions (e.g. track buffer management, host CPU functionality, and front-panel interface control) that require additional hardware with other DVD decoders, in software. In addition, support is provided for direct interfacing to a variety of industry standard DVD loaders, and also ATAPI type drives. The DVDplus firmware that forms part of the Aries 3 DVD Decoder solution is flexible and customizable ensuring rapid design of new features, upgrade ability, and a high degree of differentiation across models.

The Aries 3 DVD Decoder supports both 2D and 3D graphics with scaled video and up to 16million colors with 256 levels of transparency and scaled video, which enables the User Interfaces on Aries 3 based DVD players to be intense and compelling.

The Aries 3 DVD Decoder operates using the VM Labs NUON OS, which means that all products based on Aries 3 and the DVDplus Firmware are also optionally NUON Compatible. As such, an Aries 3 DVD Decoder based products can access and execute all content and applications created from the NUON Open Platform architecture. This allows the option of creating consumer products that offer exciting new interactive features such as 3D gaming, interactive movies, and access to html content.

A fully working NUON Compatible Aries 3 DVD player reference design is available, along with schematics, PCB layouts, and full documentation. Also available is a Graphical User Interface toolkit for Aries 3 that includes a fully customizable DVD GUI template. In addition VM Labs licenses software development tools for Aries 3 which allow third parties to customize the DVD feature-set or create proprietary applications that run on Aries 3 to allow further differentiation and enhancement of consumer DVD products.

FEATURES

- Single chip DVD processor in industry standard 208-pin PQFP or 256-pin BGA package
- Unique 4 x 128-bit parallel VLIW processor architecture specifically designed for digital video applications
- Capable of < 3000 MIPS peak performance
- Proven Aries DVD decoder architecture
- Support for DVD-Video, DVD-Audio, VCD, HDCD, CD-DA, and CD-Rom (MP3)
- Direct connection to multiple industry standard A/V loaders with support for ATAPI loaders and drives
- High quality proven DVD Navigation firmware offers excellent title compatibility
- Embedded Track Buffer processing
- Direct Front-Panel interface to VFD or micro-controller possible
- NTSC-<->PAL scaling / trans-coding
- High performance on-chip 2D and 3D graphics processing
- 16 million color, 256 levels of transparency, Graphical User Interfaces incorporating the use of scaled video
- Advanced Trick Play features including Full-Motion smooth reverse, Smooth Scan, Infinite Zoom, Picture Strobe, and Picture Enhancement
- Pan & Scan, Letterbox, and Wide-screen playback modes
- Unique DVD audio feature enhancements such as Virtual Light machine and Spectral Graphing
- Kodak Picture CD compatible
- Direct connection to memory card possible
- Dolby Digital (AC-3) Class A decode or S/PDIF output
- DTS S/PDIF output
- MPEG Multi-channel decode (to 7.1 channels)
- MP3 encode (firmware upgrade) and decode
- Karaoke functions
- Spatializer N-2-2 Virtual Surround
- Multiple GPIO support for Industry Standard Peripherals
- NUON Compatibility - Support for NUON Open Platform

SYSTEM BLOCK DIAGRAM

Figure 1 shows a typical block for an Aries 3 based DVD player -

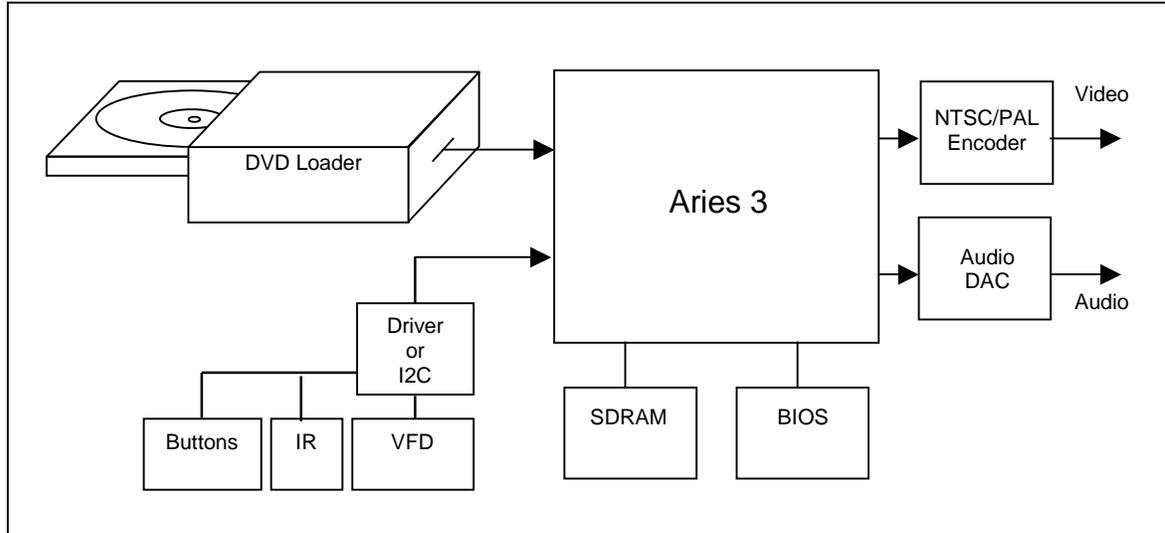


Figure 1: Aries 3 DVD System Block Diagram

INTERNAL BLOCK DIAGRAM

Figure 2 shows the internal architecture of the Aries 3 Multimedia Processor -

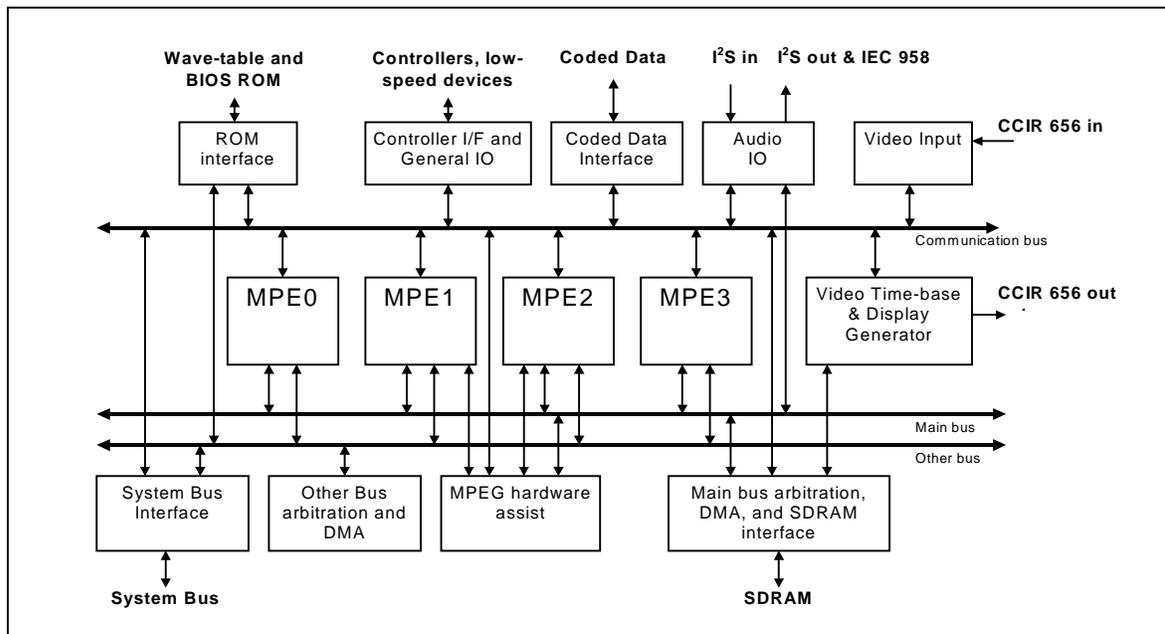


Figure 2: Aries 3 Internal Architecture

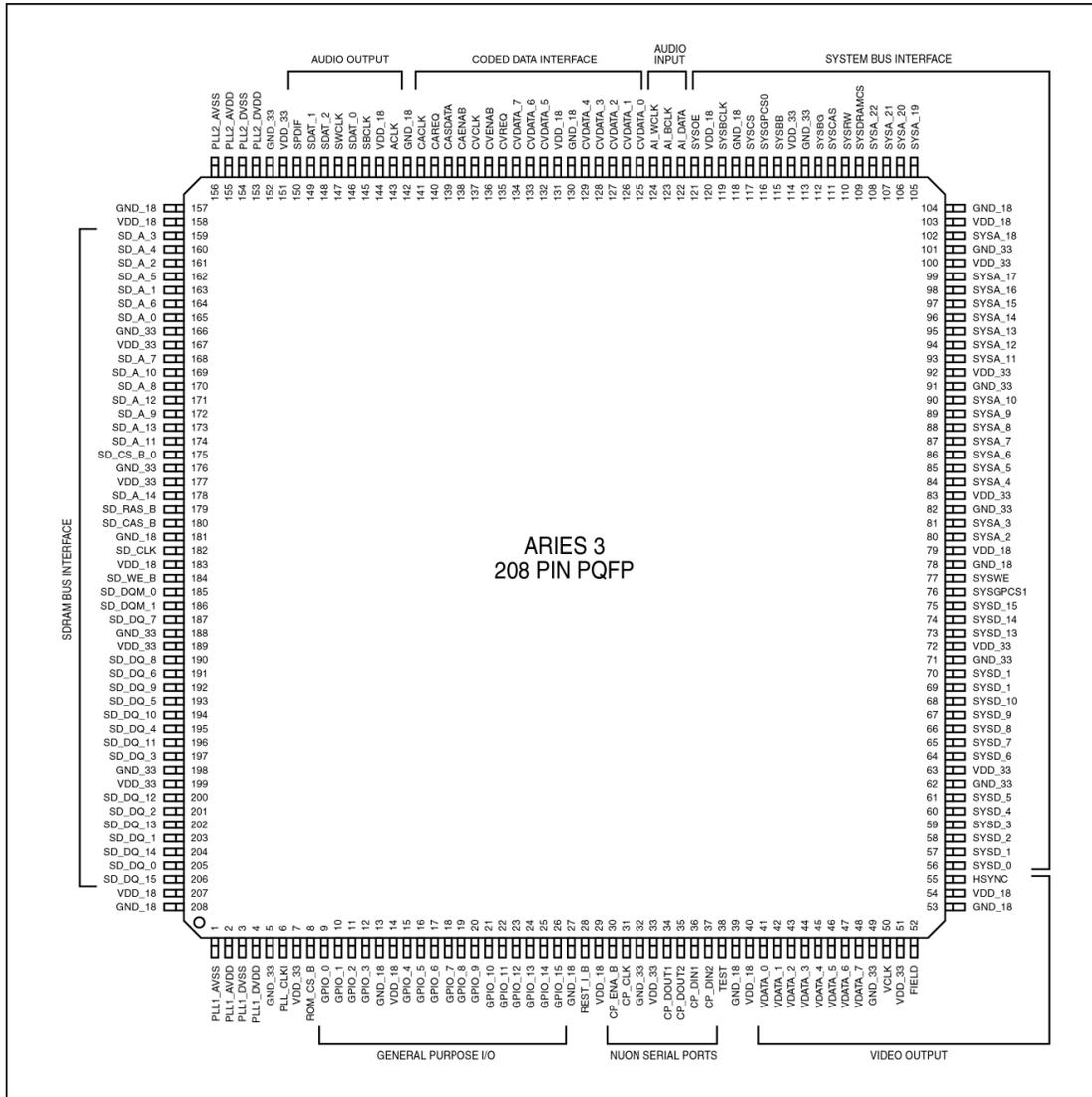
PINOUT DIAGRAM


Figure 3: Aries 3 PQFP Pinout and Function

PINOUT LIST

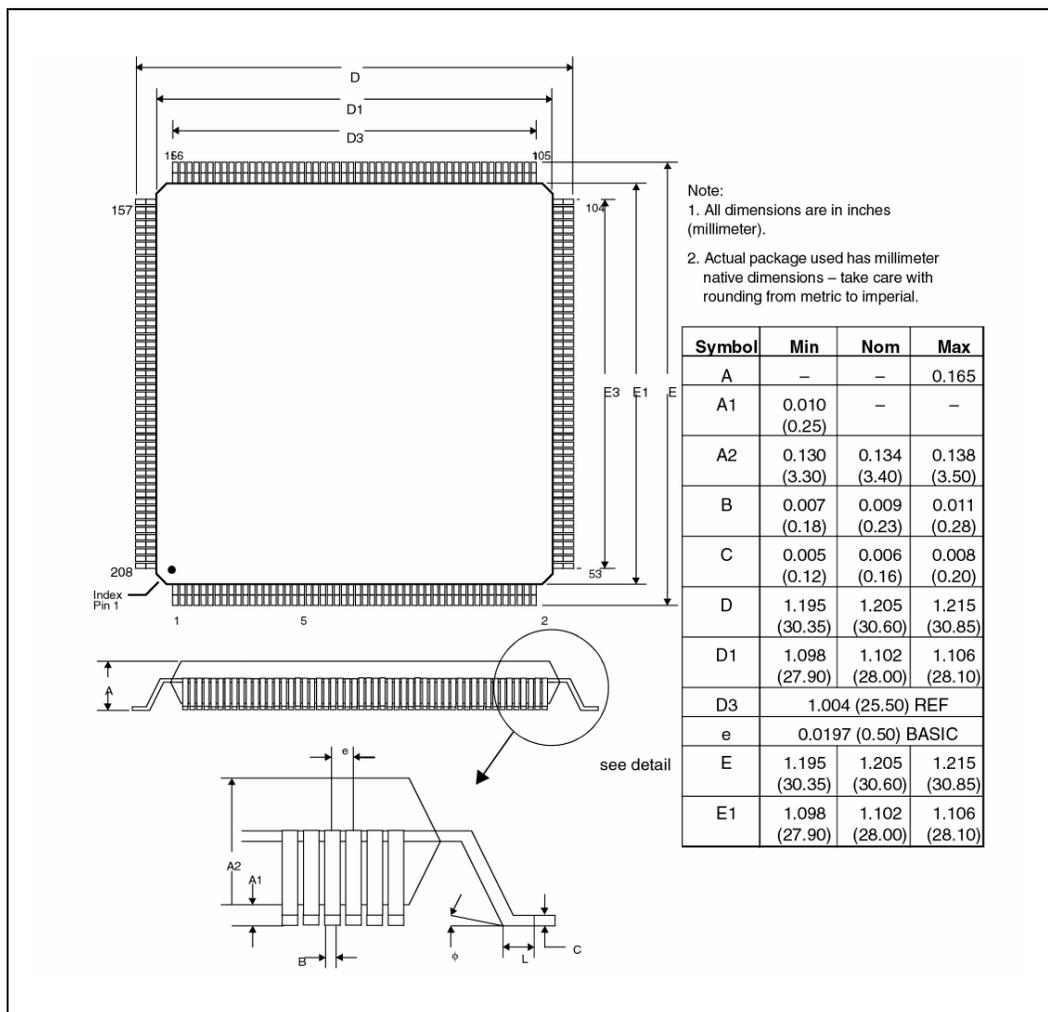
Symbol	Pins	Input/Output	Description
<i>Supplies</i>		X	
GND_18	13, 27, 39, 53, 78, 104, 118, 130, 142, 157, 181, 208	X	Processor Core Signal Ground
GND_33	5, 32, 49, 62, 71, 82, 91, 101, 113, 152, 166, 176, 188, 198	X	I/O Buffer Signal Ground

VDD_18	14, 29, 40, 54, 79, 103, 120, 131, 144, 158, 183, 207	X	Processor Core 1.8V Supply
VDD_33	7, 33, 51, 63, 72, 83, 92, 100, 114, 151, 167, 177, 189, 199	X	I/O Buffers 3.3V Supply
<i>Coded Data Interface</i>			
CVDATA[0:7]	134, 133, 132, 129, 128, 127, 126, 125	I	Coded Video/Audio Stream Data Inputs
CVENAB	136	I	Coded Video Enable for Data Strobe
CVCLK	137	I	Coded Video Stream Data Clock
CVREQ	135	O	Coded Video Stream Data Request
CAENAB	138	I	Coded Audio Enable for Data Strobe
CACLK	141	I	Coded Audio Stream Data Clock
CAREQ	140	O	Coded Audio Stream Data Request
CASDATA	139	I	Coded Audio Serial Data
<i>Audio Interfaces</i>			
ACLK	143	I	Audio Master Clock
AI_DATA	122	I	Serial Audio Data Input
AI_BCLK	123	I	Serial Audio Data Input Bit Clock
AI_WCLK	124	I	Serial Audio Data Input Word Clock
SDAT[2:0]	148, 149, 146	O	Serial Audio Data Outputs
SBCLK	145	O	Serial Audio Bit Clock Output
SWCLK	147	O	Serial Audio Word Clock Output
SPDIF	150	O	S/PDIF Audio Data Output
<i>Video Output Interface</i>			
VDATA[7:0]	48, 47, 46, 45, 44, 43, 42, 41	O	Video Data Outputs
VCLK	50	O	Video Output Clock
HSYNC	55	O	Video Horizontal Sync Pulse Output
FIELD	52	O	Video Field Sync Pulse Output
<i>NUON Serial Ports Interface</i>			
CP_DIN[2:1]	37, 36	I	NUON Serial Ports Data Inputs
CP_DOUT[2:1]	35, 34	O	NUON Serial Ports Data Outputs
CP_CLK	31	O	NUON Serial Ports Data Clock
CP_ENA_B	30	O	NUON Serial Ports Data Enable
<i>System Bus Interface</i>			
SYSD[15:0]	754, 74, 73, 70, 69, 68, 67, 66, 65, 64, 61, 60, 59, 58, 57, 56	I/O	System Bus Data Lines
SYSA[22:2]	108, 107, 106, 105, 102, 99, 98, 97, 96, 95, 94, 93, 90, 89, 88, 87, 86, 85, 84, 81, 80	I/O	System Bus Address Lines

SYSDRAMCS	109	O	DRAM Chip Select
SYSOE	121	O	DRAM Output Enable
SYSBG	112	I	System Bus Grant
SYSBB	115	I/O	System Bus Busy
SYSWE	77	I/O	System Bus Write Enable
SYSRW	110	I/O	System Bus Read/Write
SYSCAS	111	I/O	System Bus Column Address Strobe
SYSBCLK	119	O	System Bus Clock
SYSCS	117	I	System Bus Chip Select
SYSGPCS0	116	O	General Purpose Chip Select 0
SYSGPCS1	76	O	General Purpose Chip Select 1
<i>SDRAM Bus Interface</i>			
SD_DQ[15:0]	206, 204, 202, 200, 196, 194, 192, 190, 187, 191, 193, 195, 197, 201, 203, 205	I/O	SDRAM Bus Data Lines
SD_A[14:0]	178, 173, 171, 174, 169, 172, 170, 168, 164, 162, 160, 159, 163, 165	O	SDRAM Bus Address Lines
SD_DQM_0	185	O	SDRAM Data Bank Address Mask 0
SD_DQM_1	186	O	SDRAM Data Bank Address Mask 1
SD_WE_B	184	O	SDRAM Bus Write Enable
SD_CAS_B	180	O	SDRAM Bus Column Address Strobe
SD_RAS_B	179	O	SDRAM Bus Row Address Strobe
SDCLK	182	O	SDRAM Bus Clock
SD_CS_B_0	175	O	SDRAM Bus Chip Select
<i>Clock Generation</i>			
PLL_CLKI	6	I	27MHz System Clock Input
PLL1_AVDD	2	X	PLL1 Analog Signal Ground
PLL1_AVSS	1	X	PLL1 3.3V Analog Supply
PLL1_DVVD	4	X	PLL1 Digital Signal Ground
PLL1_DVSS	3	X	PLL1 3.3V Digital Supply
PLL2_AVDD	155	X	PLL2 Analog Signal Ground
PLL2_AVSS	156	X	PLL2 3.3V Analog Supply
PLL2_DVVD	153	X	PLL2 Digital Signal Ground
PLL2_DVSS	154	X	PLL2 3.3V Digital Supply
<i>Global Pins</i>			
GPIO [15:0]	26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9	I/O	General Purpose I/O Pins
ROM_CS_B	8	O	ROM Chip Select
RESETI	28	I	Reset/Reboot
TEST	38	I	Test Mode Enable

ORDERING INFORMATION

Part Number	Description	Package
Aries 3	DVD Multimedia Processor	208 PQFP


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